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L6: Entry 29 of 53 File: USPT Nov 12, 1991

DOCUMENT-IDENTIFIER: US 5065090 A
TITLE: Method for testing integrated circuits having a grid-based, "cross-check" t e

BSPR:
The present invention is a new test structure which allows up to 100 percent electrical testing of Very Large Scale Integrated Circuits by the addition of an array of test-points in the Integrated Circuit (IC). According to the broadest aspects of the present invention, the test structure consists of a multi-dimensional array of externally accessible "probe-lines" and "sense-lines" with an electronic switch at each intersection of the probe-lines with the sense-lines. The probe-lines and the sense-lines are electrically connected to external text electronics by the means of probe-points. One end of each of the electronic switches is tied to a test-point on the IC where an electrical signal is to be either measured or controlled during test and the other end of the switch is tied to a said sense-line. The ON and the OFF states of the electronic switches are controlled by probe-lines. Thus, by applying signal levels on the probe-lines one at a time and by external monitoring of the signals present on the sense-lines, the electrical test signals at every intersections of the probe-lines and sense-lines can be measured. For example, a 100.times.100, 2-dimensional, array consisting of 100 probe-lines and 100 sense-lines would allow direct testing of up to 10,000 test-points on the IC, however, requiring only 200 additional probe-points which must be connected to external test electronics through mechanical probes. This number of external probe-points can however be further reduced by accessing the probe-lines and the sense-lines through dedicated on-chip test electronics consisting of serial/parallel shift-registers on the IC being tested. Thus, further reducing the external probe-point requirement to less than 10 as compared to the 200 probe-point requirement mentioned above. Besides being able to measure the absence or the presence of a signal at a test-point, this test structure also permits the measurement of analog parameters such as voltage amplitude and current sourcing and sinking capabilities of an electronic circuit. These analog measurements give a very good measure of the speed and the noise margins of the device under test.

DRPR:
FIG. 4 integrates electronic shift-registers with the probe-lines and sense-lines to reduce the number of probe-points required to control the probe-lines and to observe the outputs of the sense-lines.

DEPR:
It is possible to reduce the number of probe-points required to excite the probe-lines and to observe the sense-lines, by including on-chip test electronics on the IC being tested. A preferred approach to on-chip test electronics is to store the information corresponding to the probe-lines and sense-lines in shift-registers on the IC being tested, as shown in FIG. 4. The outputs of the shift-register 27 control the probe-lines P1 through PN and are designed to activate only one probe-line at a time during testing. When a specific probe-line is activated, the electrical signals on the test-points connected to the switches controlled by that specific probe-line are transferred to the sense-lines S1 through SM. The signals present on the sense-line are next stored in shift-register 28 connected to the sense-lines. This is achieved by applying an external control signal to the parallel/serial control 29 to put the shift-register 28 in the parallel mode and turning the clock 30 ON once. The signals on the sense-lines are now stored in the sense shift-registers 28. Next, the signals stored in the shift-register 28 can be serially read out at probe-point 32 for analysis by external test electronics. This is achieved by

applying an external signal to the parallel/serial control probe-point 29 to put the shift-register 28 in a serial mode and turning the clock 30 ON and OFF M times. Similarly, the control data in the probe-line shift-register 27 can be loaded from external test electronics in by presenting the data in a serial manner at the input probe-point 33 and by turning the clock 34 ON and OFF N times. The input and output terminals of the shift-registers can be series connected with those of other ICs to allow simultaneous testing of multiple ICs in a large system. A comparator circuit may be inserted between the output of the sense-lines and the input to the shift-register 28 to measure the amplitudes of the signals present on the sense-lines.

DEPR:
The use of on-chip shift-registers to store the data permits the number of probe-points to be reduced from a total of N+M to about 6. In fact, a further reduction in the number of probe-points necessary to implement the "cross-check" technique can be achieved by replacing the shift-register 27 controlling the probe-lines by an on-chip circuit such as a counter that during testing would activate the probe-lines one at a time in an orderly manner without the need for external data entry.

DEPR:
The LFSR shown in FIG. 5 is made up of data storage latches 38 and Exclusive-OR gates 40. When the CLOCK 42 is turned `ON`, the output signals of the latches are Exclusive-ORed with the data present on the sense-lines 44. The outputs of the Exclusive-OR gates are stored in the following latches on the LFSR. The LFSR has a special property that it retains a signature of the past data stored in the shift-registers while it is compacted with the new data input from the sense-lines 44. Thus the sense data can be compacted in the LFSR and then read out only occasionally at the output probe-point 43. The data read out from the LFSR will carry a signature of the past data on the sense-lines and would therefore in most cases indicate if an error was detected on the sense-lines. For example, the data in the LFSR can be read out once following each cycle of testing in which all the probe-lines 46 have been excited once for a fixed input test pattern. Thus, if the test structure consists of N probe-lines, the data in the LFSR will need to be read out only once in N cycles. After the data has been read out, the input test pattern to the IC is changed and all the N probe-lines are activated once again, one at a time, without the need to read out the sense-line outputs after each probe-line activation. This procedure reduces the amount of data read by the external test electronics by a factor of N. Several other wellknown techniques can also be employed to compact the sense-line data on the IC such as, counting 1's or parity techniques. Both the LFSR and the sense-lines signals may be connected to external test equipment by the means of probe-points to allow more detailed testing.

DEPR:
The "cross-check" test structure can also be extended in the 2-dimensions to test multiple electronic components on a wafer or on a package, as shown in FIG. 7. In this case the probe-lines P1,1 thorugh P2,N2 and the sense-lines S1,1 through S2,M2 are shared between electronic components such as ICs 60. The electronic components 60 may be of different sizes in either of the two dimensions. As mentioned earlier, the on-chip probe and sense shift-registers of several different ICs can also be cascaded to test a large system consisting of several ICs.

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L6: Entry 11 of 53 File: USPT Feb 27, 1996

DOCUMENT-IDENTIFIER: US 5495486 A
TITLE: Method and apparatus for testing integrated circuits

ABPL:
Individual elements of an integrated circuit such as storage elements, (for example, latch elements), can be selectively coupled to select lines and probe lines. During normal operation the latches are not connected to the select lines and behave as a normal latch. During a write/control test operation, the latch is connected to a select line and data placed on the select line is provided to an input of latch. Thereafter, the latch is placed into a latching state in response to the probe line and the clock signal, latching the data provided from the select line into latch. In order to read/observe data, the clock line and probe line are controlled to route data onto the associated select line. In one embodiment the probe line controls a transistor switch that connects the select line to the input of the latch. The probe line also controls a transmission gate which is placed in the latch to toggle the latch between a latching condition and a non-latching condition, in response to signals on the probe line. Preferably each select line and probe line are attached to a plurality of elements and each element is connected to one select line and one probe line. Thus, by placing signals on the select line and probe line, any individual IC element can be addressed for controlling and/or observing.

BSPR:
In one embodiment, the storage elements include data latches that are selectably coupleable to associated select lines and probe lines. A first controllable switch couples the input of the data latch to the associated select line in response to a signal on the associated probe line. A second controllable switch enables storage of data in the latch in response to the probe line signal. Data which is placed on one of the select lines can be directly (i.e., without intervening storage in another storage element of the main circuitry of the IC) stored in one of the latches. Data stored in one of the latches can be output to the associated select line for direct observation (i.e., without subsequent storage in another storage element of the main circuitry of the IC). The input and output of the data is accomplished using only the associated select line and associated probe line, along with the clock input (which is provided for use during normal operation of the circuit as well).

DRPR:
FIG. 3 is a schematic depiction of the connection of sense lines and probe lines to storage elements according to one embodiment of the present invention;

DEPR:
As shown in FIG. 3, an integrated circuit 110 includes a plurality of storage elements 112a through 112l. The integrated circuit 110 also includes a plurality of gate elements, only one of which 125 is depicted in FIG. 3. A number of conductors are provided which interconnect the storage elements with each other and with the gates, only four of which 142a, 142b, 142c, 142d are depicted in FIG. 3. The design, location and interconnection of the storage elements and gates are a function of the desired operation of the integration of the circuit and the details are not depicted in FIG. 3 as these are matters known to those skilled in the art. In addition to the interconnections 142a to 142d, used during normal operation of the integrated circuit 110, each of the plurality of storage elements 112a through 112o is also connected to one of a plurality of select lines, 122a through 122d and to one of a plurality of probe lines, 124a through 124e, in a manner to be described more fully below, for use during testing of the integrated circuit. The select lines 122a through 122d are connected to an

addressing and read/write control component ARWC 126. The probe lines are connected to an addressing circuit 128. The ARWC 126 and Addressing Circuit 128 will be described more fully below. The ARWC 126 and Addressing Circuit 128 are controlled using control and data signals received either directly from peripheral input-output pads 118a through 118f or from intermediate circuitry on the integrated circuit 110 which may be addressing circuitry of a type known to those of skill in the art or as described below. The ARWC 126 and Addressing Circuit 128 also receive control and data signals from a data generator 197 which, for example, may provide pseudo-random test vectors either upon power up or in response to signals received from an external tester 199. The data on the sense line 122 can be provided from the peripheral pads, either directly or using intervening logic circuitry, or can be generated on the chip, for example, using data generator 197. The on-chip circuitry used to convey data from the peripheral pads and/or data generator and to provide the necessary clock signal are not depicted because circuitry to achieve the desired functions are known to those skilled in the art.

DEPR:
As depicted in FIG. 4, one embodiment of the present invention includes a plurality of data latches 132 each of which can be selectively coupled to an associated one of the select lines, e.g. the nth select line SL.sub.n 122 and an associated one of the probe lines such as the mth probe line PL.sub.m 124. Coupling to the associated select line 122 is by way of a controllable switch S.sub.1 134 which is controlled via a connection 136 to the associated probe line 124. In the embodiment depicted in FIG. 4, the controllable switch 134 is a field effect transistor with the source and drain contacts connected to the latch 132 and select line 122 and with the gate terminal connected to the probe line 124. Any type of switch which permits the select line to be connected to the latch 132 under control of the probe line 124 can be used. Connection of the latch 132 to the probe line 124 is by way of a transmission gate T3 138 one control line of which is directly connected to the probe line 124 the other of the control line is connected to the probe line by way of an invertor G4 140. Although an FET as a sense device and transmission gate implementation are shown, the same functionality can be obtained by substituting the depicted structure with equivalent circuits such as tri-state drivers, bi-polar or BiCMOS logic and the like. Similar control from probe line 124 may be derived from various logic gates in place of invertor G4. The latch 132 is also connected to a data input 142 for use during normal (non-test) operation of the IC. In one embodiment the data input 142 can be the output 143 of a substantially identical upstream storage element 112. The input can also be from an upstream logic gate. Connection to the data input 142 is by way of an invertor G1 144 and a transmission gate T1 146. The transmission gate T1 146 is controlled in response to a clock signal CL 148 and its inverse CL 150. Input lines for the clock signal 148 and inverse clock 150 are not depicted in FIG. 4 since these are achieved in a manner well known to those skilled in the art.

DEPR:
Normal operation (non-testing operation) will be described first. During normal operation, the probe line PL.sub.n is maintained in a "1" or high state. This places switch S1 134 in an open or "off" state. Thus, there is no pathway from the select line SL.sub.n to the latch 132 during normal operation. Because the probe line 124 is high, the transmission gate T3 138 is in an "on" state. Accordingly, during normal operation, whether the latch 132 is in a latched or non-latched state depends only on whether the transmission gate T2 156 is on or off. The state of the transmission gate T2 is controlled solely by the clock signal 148. Thus, as seen in Table I, during normal operation, when the clock is in a high "1" state, the transmission gate T1 is on and the latch 132 is in a "non-latched" condition. In the opposite clock state ("zero"), the latch 132 stores whatever data was provided at the input node 158 during the previous non-latched state and the transmission gate T1 is configured in a " off" state such that no further input from the data input line 142 will be allowed to perturb the state of the latch 132. In this way, it can be seen that when PL.sub.n equals one, the circuit depicted in FIG. 4 behaves like a normal clock-responsive latch. In order to achieve full testing, it is desired to both control or write to latch 132 and to read or observe data which is stored in the latch. The write/control test procedure involves two steps. The first step is the step of providing data on the select line as input to a latch and the second step is storing the data into the latch. As depicted in Table I, in the first step, data is provided on the select line 122, the associated probe line 124 is

provided in a low or "zero" state and the clock 148 is in a low or "zero" state. Because the probe line 124 is in a low or "zero" state, the switch S1 134 is in an "on" or conducting state. Thus, the data on the select line 122 is provided through switch S1 to the input node 158 of the gate 132. Because the clock signal is low, transmission gate T1 is "off" such that any data on data input line 142 will not perturb the state of the input node 158. The latch 132 is in a "not-latched" state since transmission gate T3 is "off".

DEPR:
In the second step, the data which was provided to the input node 158 (via switch S1 from line SL.sub.n 122) is latched in the gate 132. In order to store the data, the clock signal is maintained in the low or "zero" state. The signal on the probe line PL.sub.m 124 is changed to the "1" or high state. This causes transmission gate T3 138 to change to a conducting state thus latching the data in the latch 132. When this happens, the switch S1 changes to a non-conducting state and the test data on the select line SL.sub.n can now be changed without changing the data in the latch.

DEPR:
In order to read or observe data in an individual latch of the integrated circuit, the clock is held at a high or "1" state while the probe line 124 is held at a low or "zero" state. The select line is not actively driven during this procedure. As seen in Table I, the latch 132 is in an unlatched state because transmission gate T2 156 and T3 138 are both "off". Transmission gate T1 146 and switch S1 134 are both "on". Thus, test data from the data pin 142 is transferred to the select line 122 through gate G1 144, transmission gate T1 146 and switch S1 134. The data can then be read out through the select line. Thus, during the read/observe state, the data which is read out onto the select line is not the data from the latch 132 associated with probe line 124. Rather, it is the data which resides on the data pin 142. In one implementation, the data on the data pin 142 will be data from the "upstream" data latch. For example, referring to FIG. 3, if the write/control procedure described above is used for storing a byte of data into the latch 112b, the read/observe procedure can be used to place the data which is input into gate 112d (i.e., the data output from latch 112b) onto select line 122b.

DEPR:
In order to address the individual storage elements to perform the write/control and read operations described above, it is necessary to provide signals on the select lines and probe lines in the desired sequence. A number of options are available for providing desired signals on the select lines and probe lines as depicted in FIG. 5. In one embodiment, the probe lines PL.sub.m are addressed by an addressing circuit 128 which includes a shift register/decoder 164 and enable buffers B2 166a-166g. If it is desired to address the probe lines 124a through 124g sequentially, a "1" can be shifted through the latches 168a through 168g of the shift register 164 while holding the "test enable" lines TE for the buffers 166a through 166g in an enabling state. If it is desired to address the probe lines in a different order, a decoder circuit could be used in place of a shift register as will be apparent to those skilled in the art. The select line addressing and read/write circuit (ARWL) 126 can include a data register 172 having a plurality of latches 174a through 174e. Data can be loaded into the data register 172 in a number of ways. In the embodiment depicted in FIG. 5, data can be shifted into the data register 172 through a serial input line 173. As will be apparent to those skilled in the art, data can also be provided to the register 172 in parallel. The data which is provided to the data register 173 can be provided through the peripheral pads 118 and/or from a data generator 197 as described above. The select lines 122a through 122e are driven by buffers 176a through 176e when the write enable signal WE 178 is "on", transferring test data in the select line data register 172 to the select lines 122a through 122e. This mode is used during the write/control portion of the test procedure. During read/observe, the write enable signals 178 are "off". In this way the test signal which is placed on the select lines 122a through 122e as described above, is transmitted to the input of the data register and captured there. The test data can then be shifted out through a serial output line 180 for example to an external tester. Alternatively, the data can be compressed into a signature. e.g. using exclusive OR gates 182a-182d. The signature generation capability of the data register 172 can also be used to generate pseudo-random test vectors on the integrated circuit, e.g. according to the procedures described in Chandra, et al., "ATPG Based on a Novel Grid-Addressable Latch Element" 28th ACM/IEEE Design

Automation Conference, Paper 18.3, p 282-286, July 1991 and U.S. Pat. No. 5,206,862 issued Apr. 27, 1993 incorporated herein by reference. These on-chip generated test patterns can be written to the latches 112, resulting in a significantly reduced number of external test vectors needed to achieve the level of testing desired. A multiplexer instead of the exclusive OR gates 182a through 182d can be used if signature compression is not desired.

DEPR:
The present invention can also be used in connection with reading/observing the output from a gate such as combinational logic and gate 125 depicted in FIG. 3. As shown in FIG. 3, in positions where the latch 112 is not located at the cross-point of a sense and probe line, an observational test point 192 can be added. In the embodiment depicted in FIG. 3, the observational test point 192 includes a switch 194 controlled by a probe line 124d to controllably provide the output of the gate 125 to a select line 122c.

DEPR:
In view of the above description, a number of advantages of the present invention are apparent. The present invention permits individually directly storing to and reading from storage elements of an IC while requiring only two additional wires connected to each storage element to achieve this function. Furthermore, each of these sense wires and probe wires can be connected to a plurality of storage elements. Thus, if there are N select lines and M probe lines, the present invention permits individually controlling and observing M.times.N storage elements using M.times.N additional wires. This reduction in the number of wires for achieving this function provides a significant reduction of the IC area which must be devoted to wires for testing purposes. The circuitry achieves the desired function while requiring only a small number of additional circuit elements at each latch. Compared with previous devices, the present invention has little impact on the speed of operation of the IC during normal operation because no gates are added in series with the data path. Compared with previous devices, the present invention provides for rapid operation during test procedures because test structures do not have to be serially shifted in and out of long shift registers. Since elements of the IC can be individually controlled and/or observed, the length and number of test vectors needed to achieve a desired degree of confidence is decreased compared to, for example, the requirements of shift register testing devices. Furthermore, the amount of time and effort needed to devise and generate test vectors to achieve the desired degree of testing is decreased, compared with the shift register approach, since individual elements can be controlled and observed. On-chip test pattern generation, including pseudo-random test vector generation, significantly reduces the number of external test patterns and the required test time.

CLPR:
5. Apparatus, as claimed in claim 1, further comprising addressing means for selectively placing signals on said probe lines to connect a desired one of said plurality of data latches to a desired one of said select lines.

CLPR:
14. Apparatus, as claimed in claim 13, wherein each data latch further comprises means for storing data provided from said data input in response to a fifth signal on said clock input and a sixth signal on said associated probe line.

CLPV:
wherein, using only said associated select line, said associated probe line and said clock input, data placed on said associated select line is latched into the data latch associated therewith and data stored in the data latch associated with said associated select line is output to said associated select line.

CLPV:
providing a plurality of data latches each having a data input, a clock input, an associated select line, and an associated probe line;

CLPV:
coupling a first controllable switch between each data latch and said associated select line, said first controllable switch being responsive to a first signal on said associated probe line;

CLPV:

coupling a second controllable switch in each data latch to said associated probe line, said second controllable switch also being responsive to said first signal on said associated probe line, said second controllable switch enabling latching of data in each data latch in response to said first signal;

CLPV:
changing said first probe line to a second probe line binary state to latch the desired data into a first data latch;

CLPV:
placing said first probe line in said first probe line binary state to transmit data stored in said first data latch to said first select line.

CLPW:
a first controllable switch coupling the data input of each of said plurality of data latches to said associated one of said select lines in response to a first signal on an associated one of said probe lines;

CLPW:
wherein a second controllable switch in each data latch enables latching of data in each of said plurality of data latches in response to said first signal on said associated one of said probe lines; and

CLPW:
means for latching data into said data latch in response to a first signal on said clock input and a second signal on an associated probe line, the data being transmitted on an associated select line; and

CLPW:
means for transmitting data from said data latch to said associated select line in response to a third signal on said clock input and a fourth signal on said associated probe line.

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L11: Entry 7 of 23 File: USPT Dec 14, 1999

DOCUMENT-IDENTIFIER: US 6003142 A
TITLE: Test facilitating circuit of microprocessor

BSPR:
The test facilitating circuit may further involve a frequency doubler for doubling the frequency of an external clock signal, a frequency divider for dividing the frequency of the output of the frequency doubler, an adjuster for adjusting a fluctuation in the phase of an internal clock signal, and a clock selector for selecting the output of the frequency doubler as a clock signal to write the test program into the cache memory and read the test results from the cache memory to the outside, and the output of the frequency divider as a clock signal to run the test program to test the internal circuits of the microprocessor.

BSPR:
The test facilitating circuit may further involve a logic circuit for providing an exclusive OR of external clock signals having different phases, to generate an internal clock signal whose frequency is higher than those of the external clock signals. One of the external clock signals is used to write the test program into the cache memory and read the test results from the cache memory to the outside. The internal clock signal is used to run the test program to test the internal circuits of the microprocessor.

DEPR:
In a cache test mode, the low-speed clock signal that fits the specification of a tester (not shown) is used to write a test program into the cache memory 1 and read test results from the cache memory 1. Only when executing the test program stored in the cache memory 1, the high-speed clock signal is used so that the test is carried out at a frequency that is higher than the maximum frequency of the microprocessor to be tested. The fifth embodiment is capable of using an inexpensive tester operating at low frequencies to test a microprocessor with a high-speed clock signal.

CLPV:
a clock selector for selecting the output of the frequency doubler as a clock signal to write the test program into said cache memory and read the test results from said cache memory to the outside, and the output of the frequency divider as a clock signal to run the test program to test the internal circuits of the microprocessor.

CLPV:
a logic circuit for providing an exclusive OR of external clock signals having different phases, to generate an internal clock signal whose frequency is higher than those of the external clock signals, one of the external clock signals being used to write the test program into said cache memory and read the test results from said cache memory to the outside, the internal clock signal being used to run the test program to test the internal circuits of the microprocessor.

CLPV:
a clock selector for selecting the output of the frequency doubler as a clock signal to write the test program into said cache memory and read the test results from said cache memory to the outside, and the output of the frequency divider as a clock signal to run the test program to test the internal circuits of the microprocessor.

CLPV:

a logic circuit for providing an exclusive OR of external clock signals having different phases, to generate an internal clock signal whose frequency is higher than those of the external clock signals, one of the external clock signals being used to write the test program into said cache memory and read the test results from said cache memory to the outside, the internal clock signal being used to run the test program to test the internal circuits of the microprocessor.

CLPV:
a clock selector for selecting the output of the frequency doubler as a clock signal to write the test program into said cache memory and read the test results from said cache memory to the outside, and the output of the frequency divider as a clock signal to run the test program to test the internal circuits of the microprocessor.

CLPV:
a clock selector for selecting the output of the frequency doubler as a clock signal to write the test program into said cache memory and read the test results from said cache memory to the outside, and the output of the frequency divider as a clock signal to run the test program to test the internal circuits of the microprocessor.

CLPV:
a logic circuit for providing an exclusive OR of external clock signals having different phases, to generate an internal clock signal whose frequency is higher than those of the external clock signals, one of the external clock signals being used to write the test program into said cache memory and read the test results from said cache memory to the outside, the internal clock signal being used to run the test program to test the internal circuits of the microprocessor.

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L9: Entry 8 of 15 File: USPT Oct 20, 1987

DOCUMENT-IDENTIFIER: US 4701696 A
TITLE: Retargetable buffer probe

DEPR:
Referring to FIG. 1, a data acquisition system 10, illustrated in block diagram form, is adapted to acquire and store in a random access acquisition memory 12, a sequence of data, address and selected control line states of a microprocessor operating in conjunction with system under test 14. System 10 comprises probe 16, according to the present invention, which connects the data, address and a selected portion of control lines appearing on the pins of the microprocessor under test to data, address and control latches 18, 20 and 22, through internal buffers and cross-connect wiring in the probe and lines 19, 21 and 23 respectively. Probe 16 also connects other selected control lines appearing at the pins of the microprocessor to the input of transaction analyzer 26 over lines 34.

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USPT	l1 same l5	53	L6
USPT	l2 or l3 or l4	700970	L5
USPT	scan	120545	L4
USPT	shift adj1 register	45280	L3
USPT	storage or latch	623294	L2
USPT	probe adj1 line	354	L1

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L9: Entry 4 of 15 File: USPT Jul 6, 1993

DOCUMENT-IDENTIFIER: US 5226092 A
TITLE: Method and apparatus for learning in a neural network

CLPR:
15. A method for correcting pattern recognition error in a computer that is configured as an artificial neural network, said artificial neural network comprising a plurality of interconnected processing units arranged in layers including an input layer, a second layer connected to the input layer, and an output layer, each processing unit being arranged to accept a plurality of inputs and provide an output according to a pre-determined activation function, each of the plurality of inputs being weighted according to a predetermined set of interconnection weight values and each weight value in the set being associated with a connection between the processing units in the artificial neural network, the set of interconnection weight values being stored in a memory coupled to the computer as a set W capable of being represented as a vector W, the artificial neural network being arranged to accept, in the input layer, an input pattern comprising a first data set stored in the memory, process that input pattern in a forward pass of the artificial neural network according to the pre-determined activation functions, set of weight values and corresponding interconnections, and map the input pattern to an actual output pattern comprising a second data set stored in the memory, the artificial neural network also being arranged to accept as input a desired output pattern comprising a third data set stored in the memory to be used to determine the pattern recognition error for the input pattern by computing the sum of the squared differences between the actual and desired output patterns and storing the result as an error value E, the interconnection weight values and error value E capable of being mapped to a point WE on a weight space terrain, the weight space terrain comprising a space determined by a set of all possible interconnection weight values mapped against a set of all possible error values by mapping those weight values for a given input pattern through the set of interconnected processing units of the artificial neural network using the pre-determined activation functions and taking that output pattern and computing the sum of the squared differences between the actual and desired output patterns, said weight space terrain having features of local and global minima values and identifiable ravines, the ravines comprising a discernable path to a local or global minimum value, with a path from the point WE to a local or global minimum value capable of being calculated as a gradient through a backpropagation technique, the gradient capable of being represented by a set of delta W values, the delta W values comprising a representation of the slope and the direction of the gradient and capable of being represented by a vector delta W, the gradient being used as a probe line for determining different points in the weight space and comparing them for a reduced error value E, the method for correcting pattern recognition error in the artificial neural network comprising the steps of:

CLPR:
20. A method for correcting pattern recognition error in a computer that is configured as an artificial neural network, said artificial neural network comprising a plurality of interconnected processing units arranged in layers including an input layer, a second layer connected to the input layer, and an output layer, each processing unit being arranged to accept a plurality of inputs and provide an output according to a pre-determined activation function, each of the plurality of inputs being weighted according to a predetermined set of interconnection weight values and each weight value in the set being associated with a connection between processing units in the artificial neural network, the set of interconnection weight values being stored in a memory coupled to the computer as a set W capable of being represented as a vector W, said artificial

neural network being arranged to accept, in the input layer, an input pattern comprising a first data set stored in the memory, process that input pattern in a forward pass of the artificial neural network according to the pre-determined activation functions, set of weight values and corresponding interconnections, and map the input pattern to an actual output pattern comprising a second data set stored in the memory, said artificial neural network also being arranged to accept as input a desired output pattern comprising a third data set stored in the memory to be used to determine the pattern recognition error for the input pattern by calculating and storing in the memory the sum of the squared differences between the actual and desired output patterns as an error value E, said interconnection weight values and error value E capable of being mapped to a point WE on a weight space terrain, said weight space terrain comprising a space determined by a set of all possible interconnection weight values mapped against a set of all possible error values by mapping those weight values for a given input pattern through the plurality of interconnected processing units of the artificial neural network using the pre-determined activation functions and taking that output pattern and computing the sum of the squared differences between the actual and desired output patterns, said weight space terrain having features of local and global minima values and identifiable ravines, said ravines comprising a discernable path to a local or global minimum value, with a path from the point We to a local or global minimum value capable of being calculated as a gradient through a backpropagation technique, the gradient capable of being represented by a set of delta W values, said delta W values comprising a representation of the slope and the direction of the gradient and capable of being represented by a vector delta W, the gradient being used as a probe line for determining different points in the weight space and comparing them for a reduced error value E, each probe point represented by a different distance value d away from the point WE, the correction method being a technique to adjust the set of interconnection weight values stored in the memory for the artificial neural network to be the weight values in the weight space terrain corresponding to the probe point with the lowest error value E, the d value of that probe point being considered a learning step taken in adjusting the interconnection weight values of the artificial neural network, the method for correcting pattern recognition error in the artificial neural network comprising the steps of:

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L6: Entry 3 of 53 File: USPT Nov 17, 1998

DOCUMENT-IDENTIFIER: US 5838163 A
TITLE: Testing and exercising individual, unsingulated dies on a wafer

DEPR:
As shown in FIG. 4 of the aforementioned U.S. Pat. No. 4,749,947, (reproduced herein as FIG. 11) it is possible to reduce the number of cross-check connections, per die, vis-a-vis the actual number of cross check lines traversing the die. As noted therein, a shift register (27) can be used to control a plurality of probe-lines, and are designed to activate only one probe-line at a time during testing. Another shift register (28) is connected to the sense-lines. Activating one probe line causes signals to be impressed on all of the sense lines--hence the sense line shift register (28) is operated in a parallel mode to fetch and store information from the sense lines, and is then operated in a serial clocked mode to transfer the signals from the sense lines out serially to a single probe point (32). This whole schema of reducing the test points from a one-to-one correspondence, to the number of probe and sense lines requires essentially only one connection for all of the probe lines, one connection for all of the sense lines, plus a few clock and control connections that is not related to the number of probe and sense lines.

DEPR:
The 4,749,947 patent also suggests further reduction in the number of probe points necessary to implement the cross check technique, by replacing the shift register (27) controlling the probe lines with an on-chip circuit such as a counter that during testing would activate the probe lines one at a time in an orderly manner without the need for external date entry (see column 8, lines 55-63).

DEPR:
FIG. 10a shows an example of using shift registers for selectively connecting a limited number of signals to a relatively large number of dies on a wafer. In this example, an artificially small number of dies (four dies shown: 1002a, 1002b, 1002c, and 1002d) and an artificially small number of probe and sense lines per die are shown (four probe lines P\`x\` per die, grouped in sets of four 1010\`x\`, and four sense lines S\`x\` per die, grouped in sets of four 1020\`x\`) are presented for illustrative clarity. On a typical wafer, a substantially number of dies, probe line and sense lines would be used. A plurality of sets of probe lines (1010a and 1010b shown), each set sufficient for probing any given die (one of 1002a, 1002b, 1002c, or 1002d) on the wafer, are disposed in the scribe lines, and another plurality of sets of sense lines 1020, again each set sufficient for accessing the sense lines of any individual die, are also disposed in the scribe lines.

DEPR:
A probe shift register 1030 is provided, the outputs of shift register 1030 driving the probe lines. The shift register 1030 is of the SIPO (Serial in-Parallel out) type, whereby data presented on a "DATA INPUT" line 1032 to the DI (data in) input of shift register 1030 is clocked into shift register 1030 by a "SHIFT IN" clock signal presented on a line 1034 to the clock (>) input of shift register 1030. As the "DATA IN" signal is clocked in, its data values are shifted serially along shift register outputs Q.sub.0-7 and placed on sets of probe lines 1010, connected thereto.

DEPR:
In this manner, the number of interface signals (probe and sense signals) is reduced to five, for virtually any number of dies. For more dies, sense lines and

probe lines, longer shift registers 1030 and 1040 are used.

DEPR:
FIG. 10c shows a further efficiency improvement in this method of reducing test connections through the use of shift registers. The number of dies has been artificially reduced for illustrative clarity. A typical application would have a large number of dies. Four dies (1002a', 1002b', 1002c' and 1002d') are shown, similar to dies 1002`x` in FIGS. 10a and 10b, except that these dies employ the cross-check shift register scheme referred to in U.S. Pat. No. 4,749,947, thus reducing the number of probe and sense lines per die substantially. In the Figure, three probe lines and three sense lines are shown per die (not substantially different from the actual number likely for such an application, as opposed to a significantly larger number where the die probe/sense grid is simply extended over the die). Die 1002a' is shown as typical of the remainder of the dies (1002b', 1002c' and 1002d') having three probe points 1003 and three sense points 1004. In the Figure, probe points 1003 are joined (by lines 1010') in a columnar fashion, which sense points 1004 are joined in a row-oriented fashion (by lines 1020'). In a manner similar to that shown in FIGS. 10a and 10b, probe lines 1010 are driven by a SIPO shift register 1030a having a data input signal on a line 1032 and a shift in clock signal on a line 1032. Also similar to the scheme shown in FIGS. 10a and 10b, the sense lines 1020' are connected to the data inputs of a PISO shift register 1040a, which has a load input on a line 1046, a shift clock input on a line 1044, and a data output on a line 1042. Note that the external interface (non-probe and non-sense connections to the shift registers) is identical to that of FIGS. 10a and 10b, even though the interfaces to the dies are different. While there will be differences in the meaning of the data applied at "DATA IN" and data output on "DATA OUT", between FIG. 10c and FIGS. 10a and 10b, the physical interface is identical.

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L6: Entry 5 of 53 File: USPT Aug 25, 1998

DOCUMENT-IDENTIFIER: US 5799021 A
TITLE: Method for direct access test of embedded cells and customization logic

ABPL:
Methods and related structures for both operating and testing an integrated circuit constructed of combinations of customization logic and embedded cells. Functional modes include an operational mode and a test mode with two submodes. Test terminals of embedded cells, as well as test points in customization logic, are both accessed via a multiplexing scheme using test points of x-y (row and column) wiring traces of a grid-based "cross-check" test structure for both logic testing and embedded cell testing. Common conductors or traces can be used to operate the embedded cells and to control the made and test the embedded cells and customization logic. The x and y lines can be operated as signal lines, as probe lines, as sense lines and as control lines, as needed, using multiplexing according to the invention. In addition, the x and y lines can be used, in connection with analog multiplexers and switches, to probe, stimulate and sense embedded analog signal circuits, subsystems and conditions of an embedded cell. In a case where multiple probe lines are active, test points are held in a high impedance state by placing the clock of latches or flip flops at the intersections of the sense lines and the probe lines in a suspended state and applying only half the switching voltage to the line operative as the sense line. Such latches also permit testing in the presence of asynchronous signals.

BSPR:
One form of embedded testing of VLSI circuitry is based on the use of a grid of test points at the intersections of x and y (row and column) conductive lines overlaying a VLSI "cloud" of circuitry integrated into a chip. Reference is made to U.S. Pat. No. 4,749,947, issued Jun. 7, 1988, entitled GRID-BASED, "CROSS-CHECK" TEST STRUCTURE FOR TESTING INTEGRATED CIRCUITS, inventor Tushar Gheewala for background. Referring to FIG. 1, there is shown a prior art grid-based, "CrossCheck.RTM." test structure 10 used in methods for testing random logic circuits in an integrated circuit, as disclosed in U.S. Pat. No. 4,749,947 owned by the assignee of the present invention. Therein, a grid 12 of test points 14 is accessed by addressable sets of X and Y wiring traces with the Y direction therein for sense lines S.sub.1 . . . S.sub.N and with the X direction for probe lines P.sub.1 . . . P.sub.N Traces functioning as probe lines P.sub.1 . . . P.sub.N select which row (column) of test points 14 is to be accessed, and the sense lines S.sub.1 . . . S.sub.N read the signal from the selected column (row). In one known embodiment of the prior art, the signals applied through a single input port or pin 31 are applied to the sense lines S.sub.1 . . . S.sub.N through shift register 28, and data read from the test points 14 by the sense lines S.sub.1 . . . S.sub.N are fed to a shift register 28 from which the data can be read out through a single input/output (I/O) pin or pad 32, thus minimizing the number of pins which must be dedicated to diagnostics. Because only one port was available to extract data, thus slowing down throughput, one solution suggested has been the use of a linear feedback shift register (LFSR) as a means to compress the data and to generate a signature representation of the data. Because some diagnostically useful information is lost in an LFSR, a need has existed to improve on the prior art techniques.

DEPR:
Referring to FIG. 2, this invention solves problems of the prior art of grid-based testing of an integrated circuit 110 by providing in its design direct access to sense lines S.sub.1 . . . S.sub.N and probe lines P.sub.1 . . . P.sub.N for testing both grid-based customization logic 112 and embedded cells 114 by use of first multiplexers (X) 118 at input/output ports or pads 120, 140 of an

integrated circuit between the signal lines (not shown) and grid lines 160, 180 serving as the sense lines S.sub.1 . . . S.sub.N and probe lines P.sub.1 . . . P.sub.N, and also by providing multiplexers 122 adjacent the test terminals of embedded cells 114 in the circuit design also serving as switches between signal lines and the same sense line/probe lines. Two types of circuitry are represented on the integrated circuit 110: customization logic elements 112 and embedded cells 114. Embedded cells 114 are precharacterized circuit designs which generally require a test methodology different from that of the surrounding circuitry. Embedded cells 114 are not designed at the outset for testability from the periphery of the layout area. On the other hand, grid-based testing employs probe lines P.sub.1 . . . P.sub.N to select elements of customization logic to test, and it also employs sense lines S.sub.1 . . . S.sub.N to supply excitation signals and/or observe responses to excitation signals. In accordance with a specific aspect of the invention, a latch and preferably a specific type of latch, herein referred to as a suspendable state latch 200, is designed into the customization logic 112 to connect with intersections of grid lines 160 and 180 to access test points 115 in the customization logic. The suspendable state latch 200 is preferably controllable by a clock input 116 (accessed by clock traces--not shown). A more complete description of one embodiment of a suspended state latch in accordance with the invention is found in U.S. patent application Ser. No. 07/929,873 filed Aug. 11, 1992 in the name of Tushar Gheewala entitled METHOD AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT, the description of which is incorporated herein by reference. These suspended state latches can receive at least two inputs and can provide at least two outputs, one of the ports 261 being bidirectional.

DEPR:
FIG. 3 shows the connections of sense lines 160 and probe lines 180 to pads 120 and 140 through multiplexers 118. The multiplexing switches 118 are controlled by a Chip Test Enable signal applied via test pad 185 on line 125. The Chip Test Enable signal also controls an input state retention latch 131, as hereinafter explained.

DEPR:
In either test submode, Test Enable (125) is turned ON, the input data on input pads 140 are latched into the state retention latches 131, and typically all test lines 160, 180 are connected through multiplexers 118. Test patterns can now be applied to or observed from sense and probe lines 160, 180 now connected directly to the signal pads 120 and 140 at the edge of the chip 110.

DEPR:
FIG. 3 further illustrates the specific test submodes. To test customization logic in the first test submode, only the chip test enable signal 125 needs to be active. This in turn connects input/output pads 120, 140 to sense lines 160 and probe lines 180 through switches 118. The external inputs to the operational circuit 112 are held by state retention latches 131. To test an internal circuit, for example 212, signals can now be applied to the internal suspendable state latches 200 using probe lines 180 and sense lines 160. Thus in the first test submode, the input/output pads are used to control and observe sense and probe lines, which in turn control internal storage elements to apply test patterns to internal circuits and also to observe the resulting signals to check if the circuit has any defects in it. The internal test points are located at the intersections of the sense and probe lines, where the suspendable state latches are also located. In a compact design, the test points are embedded in the suspendable state latches 200 to be activated selectively to observe output lines 170, 171. (However, the test points need not be located exclusively at the latches. There may be additional test points, such as observation points on the chip. All test points need not be at suspendable state latches. In certain applications, simple multiplexers might be satisfactory sites of test points. Since a chip design is expected to take into account at some level the nature of the test structures, adaptations of a basic test structure design are contemplated.)

DEPR:
Specifically, it may be noted that in the first test submode (test of customization logic), sense lines 160 are used both for writing into suspendable state latches 200 and for reading from the suspendable state latches 200 whereas the probe lines 180 are used only to select the suspendable state latches 200 for access through sense lines 160. In contrast during the second test submode (test

of embedded cells) sense lines 160 and probe lines 180 may be used for conducting test signals from input/output pads 120, 140 into the cell under test as well as for conducting test responses from the cell to pads 120, 140. In order to be able to access suspendable state latches and embedded cells during test, the sense and probe lines may be physically routed around, over or through the embedded cells 114.